Single-Event Upset and Scaling Trends in New Generation of the Commercial SOI PowerPC Microprocessors

Farokh Irom, Farhad Farmanesh and Coy K. Kouba

***Abstract*— Single-event upset effects from heavy ions are measured for Motorola silicon-on-insulator (SOI) microprocessor with 90 nm feature sizes. The results are compared with previous results for SOI microprocessors with feature sizes of 130 and 180 nm. The cross section of the 90 nm SOI processors is smaller than results for 130 and 180 nm counterparts, but the threshold is about the same. The scaling of the cross section with reduction of feature size and core voltage for SOI microprocessors is discussed.**

***Index Terms*— Cyclotron, heavy ion, microprocessors, silicon on insulator.**

I. Introduction

In recent years there has been interest in the possible use of unhardened commercial microprocessors in space because of their superior performance compared to hardened processors. However, unhardened devices are susceptible to upset from space radiation. More information is needed on how complex ASICs respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, which are designed with lower clock frequencies and higher internal core voltages than recent devices [1-6].

A basic method for improving the SEU immunity without degrading the performance is to reduce the SEU-sensitive volume. This can be accomplished through the use of silicon-on-insulator (SOI) substrates. For SOI processes the charge collection depth for normally incident ions is reduced by more than an order of magnitude compared to similar processes fabricated on epitaxial substrate. Because of the much smaller charge collection depth, the single-event upset (SEU) sensitivity of SOI devices is expected to be much better. However, other factors, such as lower operating voltages, reduced junction capacitance and amplification by parasitic bipolar transistors [7] may limit the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors.

The trend for commercial Silicon-on-insulator (SOI) microprocessors is to reduce feature size and internal core voltage and increase the clock frequency. Commercial microprocessors with the PowerPC architecture are now available that use partially depleted SOI processes with feature size of 90 nm and internal core voltage as low as 1.0 V and clock frequency in the GHz range.

Previously, we reported SEU measurements for SOI commercial PowerPCs with feature sizes of 180 and 130 nm [8, 9]. The results showed an order of magnitude reduction in saturated cross section compared to CMOS bulk counterparts.

This paper examines SEUs in the advanced commercial SOI microprocessors, focusing on SEU sensitivity of D-Cache, registers and hangs with feature size and internal core voltage. Results are presented for the Motorola SOI processor with feature sizes of 90 nm and internal core voltages of 1.3 and 1.0 V at maximum clock frequency of 1.6 GHz. These results are compared with results for the Motorola SOI processors with feature size of 180 and 130 nm and internal core voltages of 1.6 and 1.3 V, respectively. The scaling of the cross section with reduction of feature size and core voltage dependence for SOI microprocessors is discussed.

II. Experimental Procedure

A. Device Descriptions

The Motorola 7448 PowerPC is fabricated with SOI technology. It uses a partially depleted technology without body ties. It has a feature size of 90 nm with a silicon film thickness of 40 nm and internal core voltage of 1.3 V. A low-power version of this processor operates with an internal core voltage of 1.0 V.

The older Motorola 7457 SOI PowerPC has a feature size of 130 nm with a silicon film thickness of 55 nm and internal core voltage of 1.3 V. A low-power version of this processor operates with an internal core voltage of 1.1 V. Also, the Motorola 7455 SOI PowerPC has a feature size of 180 nm with a silicon film thickness of 110 nm and internal core voltage of 1.6 V. A low-power version of this processor operates with an internal core voltage of 1.3 V. All devices are packaged with “bump bonding” in flip-chip ball-grid array (BGA) packages.

Manuscript received July, 14 2006. The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program.

F. Irom is with the Jet Population Laboratory, California Institute of Technology, Pasadena, CA 91109 (telephone: 818-354-7463, e-mail: farokh.irom@jpl.nasa.gov.

F. F. Farmanesh is with the Jet Population Laboratory, California Institute of Technology, Pasadena, CA 91109 (telephone: 818-353-5498, e-mail: farhad.f.farmanesh@jpl.nasa.gov.

Coy K. Kouba, Johnson Space Center, Houston, TX 77058 (USA), phone: 281-483-8069, fax: 281-483-6297, email: coy.kouba-1@nasa.gov.

It is important to note that the core voltage used in our tests is the specific core voltage designed by the manufacturer for the specific product. We do not know what specific changes have been made to the processor design or the design of the internal transistors to produce devices that will work reliably with such low voltages.

Table I summarizes the recent SOI generation of the PowerPC family. The feature size is reduced from 180 to 90 nm, with core voltage reduced from 1.6 to 1.0 V. The maximum operating clock frequency ranges from 800 to 1600 MHz.

Table I. Summary of Motorola's PowerPC Family of SOI Processors.

SOI PowerPC	Feature Size (nm)	Core Voltage (V)	Maximum Operating Frequency (MHz)
7455	180	1.6	1000
7455*	180	1.3	800
7457	130	1.3	1200
7457†	130	1.1	1000
7448	90	1.3	1600
7448††	90	1.0	1000

*This is a special low power version of the Motorola SOI PowerPC7455.
†This is a special low power version of the Motorola SOI PowerPC 7457.
††This is a special low power version of the Motorola SOI PowerPC 7448.

B. Experimental Methods

Radiation testing was done at the Texas A&M University cyclotron. This facility produces the long-range ions needed for SEU testing through thick materials. Particularly, the 40 MeV/amu beams have enough range that makes it possible to do irradiations in air rather than in vacuum. The ion beams used in our measurements are listed in Table II. Both ions have enough range to penetrate the die. The LET range of 1.7 to 15 MeV-cm^2/mg was covered in the measurements. All irradiations were done using ions with normal incidence. Because of the "flip-chip" design of the Motorola PowerPC, irradiation was done from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. The thickness of the die is about 850 μm.

Radiation testing was done in air using a commercially available evaluation boards manufactured by Motorola for each processor type. This eliminated the engineering effort required to design a custom test board for the processor, and also provided a basic PROM-based system monitor instead of a complex operating system. This provides better diagnostics and control of processor information during SEU testing compared to more advanced operating systems. The external communication channel on the evaluation boards was a simple serial connection and it was used as a terminal.

The test methodologies used to measure upset errors in the D-cache, registers and hangs are discussed in detail in [1, 8, and 9] and briefly described in the following sections. Tests were performed on two to three samples for each processor type.

Table II. List of the ion beams used in our measurements.

Ion	Energy per Nucleon (MeV/amu)	Initial LET (MeV-cm^2/mg)	Range (μm)
^{20}Ne	40	1.7	1648
^{40}Ar	40	3.8	1070

1- D-cache measurement

The cache was initialized under specified condition prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from the contents of the cache, was placed in the external memory space covered by the cache. Comparing the cache contents after irradiation provided verification of the cache contents. Upsets in the cache were counted with special post beam software.

2- Registers measurement

In testing the register, the processor performs a one-word instruction infinite loop interrupted briefly every half-second to write a register snapshot to a strip chart in the physical memory. After the irradiation has ended, an external interrupt triggered a reporting routine to download the strip chart and compared the register contents with the pattern initially loaded, and counted state changes in the register.

3- Hangs measurement

We define a hang as a complex functional error where the processor operation is severely disrupted during the irradiation. We detected hangs by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, it was still operational to the point where normal software could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a hang. In nearly all cases, it was necessary to temporarily remove power from the device in order to recover and reboot the device. The analysis of hangs is complicated by the fact that one is not sure how much beam was delivered to the device before the hang occurred.

In order to roughly scope problems with hangs, we calculated the hang cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed hangs. This was done for each LET.

III. Test Results

1- Scaling Trends

A. Register Tests

Figure 1 show results of the SEU cross section measurements of the Floating Point Registers (FPR) for the Motorola PowerPC 7448 (feature size 90 nm). The measurements were done for "0" to "1" and "1" to "0" transitions. The cross sections for the two logic directions are different. We have reported similar asymmetry in registers for other SOI PowerPCs from Motorola and IBM [8].

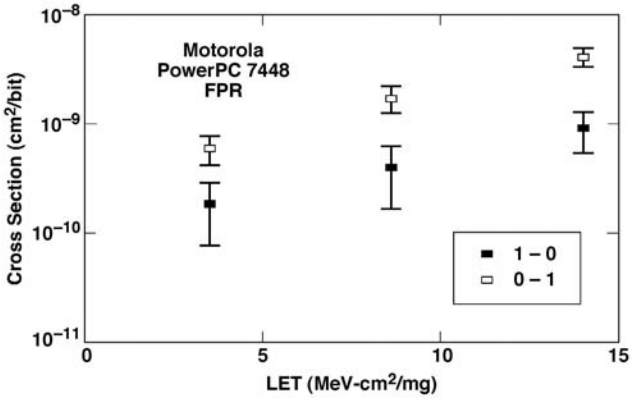

Fig. 1 SEU cross-sections for FPR of the Motorola SOI PowerPC 7448 for "1" to "0" and "0" to "1" transitions. The dashed and solid curves are only guides for the eye.

Figure 2 compares results of the SEU measurements for FPR of the Motorola PowerPC 7448 (90 nm feature size) to the results of the Motorola PowerPC 7455 (180 nm feature size). The core voltage for both measurements was 1.3 V. The SEU cross section for the Motorola PowerPC 7448 is smaller than the one for the Motorola PowerPC 7455.

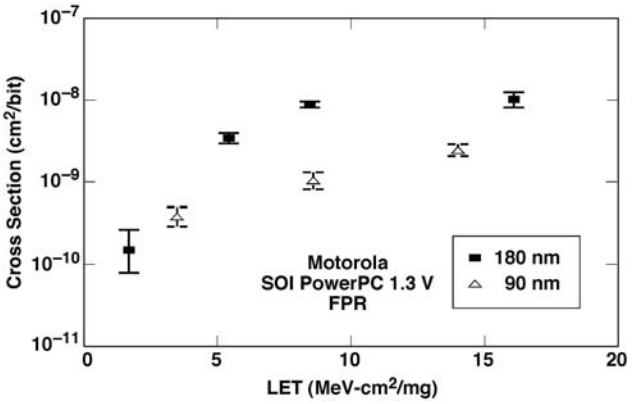

Fig. 2 Comparison of SEU cross-section for the FPR of the Motorola 7455 and 7448 PowerPC's. The dashed and solid curves are only guides for the eye.

B. Data Cache

Figure 3 compares results of the SEU measurements for D-Cache of the Motorola PowerPC 7448 (90 nm feature size) to the results of the Motorola PowerPC 7457 (130 nm feature size). Also, for comparison the results of the Motorola PowerPC 7455 (180 nm feature size) is shown. The core voltage for three measurements was 1.3 V. Even though the Motorola PowerPC 7448 processor has a much smaller feature size than the PowerPC 7455 and 7457, the LET threshold (LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of $1x10^7$ ions/cm^2) is likely not very different. The LET threshold of the SOI PowerPC processors is about 1 MeV-cm^2/mg. The saturation cross section of the Motorola PowerPC 7448 is more than a factor of 5 lower than that of the other PowerPC processors with feature sizes of 130 and 180 nm. It is interesting to note that there is little difference between the saturated cross section for SOI PowerPCs with feature size of 130 and 180 nm given the difference in feature size. These results suggest that scaling between 180 and 130 - nm feature size has little effect on SEU sensitivity. However, this trend did not continue as device feature size is changed to 90 nm. The scaling of the saturated cross section with feature size in SOI processors will be discussed further in Section IV.

The large number of storage locations within the data cache allows more statistically significant numbers of be measured, decreasing the error bars due to counting statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. Contrary to FPR results the D-Cache SEU cross section for "1" to "0" transitions is the same as that for "0" to "1" transitions.

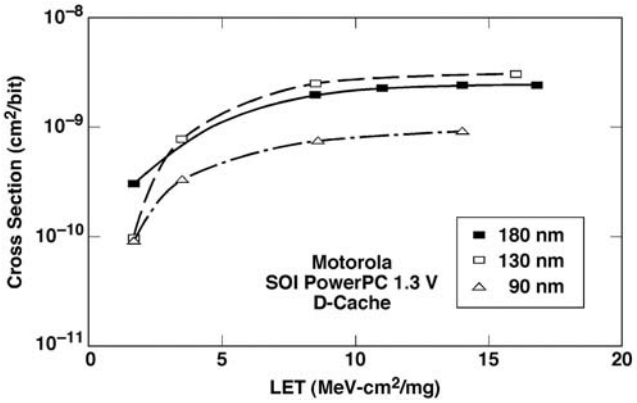

Fig. 3 Comparison of SEU cross-section for the D-Cache of the Motorola 7455, 7457 and 7448 PowerPC's. The core voltage for three measurements was 1.3 V. The dashed and solid curves are only guides for the eye.

C. Functional Errors ("Hangs")

Figure 4 compares estimated cross sections for hangs for the Motorola PowerPC 7448 (90 nm feature size) to those for the Motorola PowerPC 7457 (130 nm feature size). Also, for comparison the estimated cross section for hangs for the Motorola PowerPC 7455 (180 nm feature size) is shown. The core voltage for all three measurements was 1.3 V. Contrary to the results for the SEU measurements of the D-Cache and the FPR there are no differences between results of three measurements. These results suggest that scaling between 180

and 90 - nm feature size has little effect on hangs if internal core voltage stays the same.

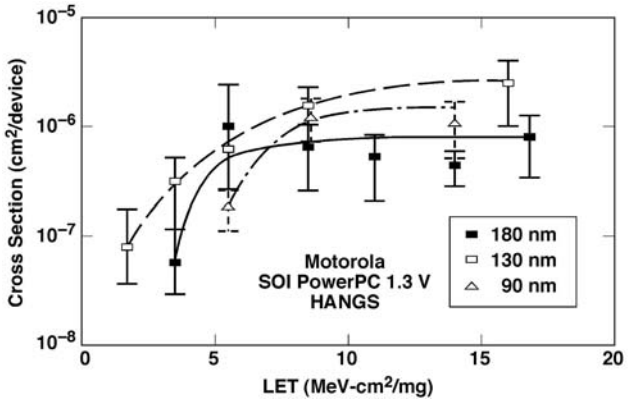

Fig. 4 Comparison of estimated hangs cross-section for the Motorola 7455, 7457 and 7448 PowerPC's. The core voltage for three measurements was 1.3 V. The dashed and solid curves are only guides for the eye.

2- Core Voltage

A. D-Cache

Figure 5 shows results of the SEU measurements for D-Cache of the Motorola PowerPC 7448 (90 nm feature size) at two internal core voltages of 1.3 and 1.0 V. The SEU measurements for the part designed with lower internal core voltage, 1.0 V, is slightly larger than the one for the operating voltage of 1.3 V.

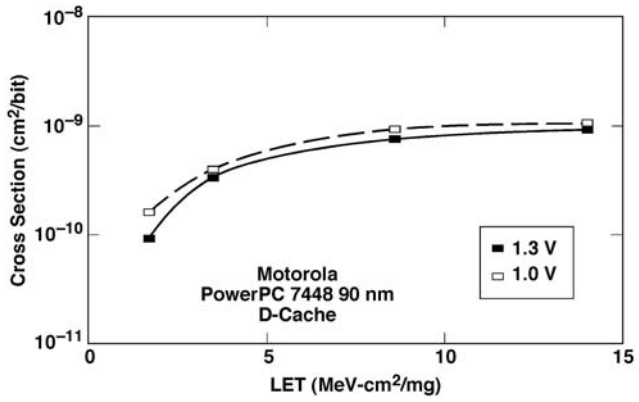

Fig. 5 Comparison of SEU cross sections for D-Cache for Motorola PowerPC 7448 for internal core voltage of 1.3 and 1.0 V. The dashed and solid curves are only guides for the eye.

Previously, we have studied the core voltage dependence of the SEU measurements for D-Cache on the Motorola PowerPCs 7455 and 7457 [10]. Figure 6 compares results of the previous SEU measurements of the D-Cache of the Motorola PowerPC 7457 with a core voltage of 1.3 V to the results of the Motorola PowerPC 7457 with a core voltage of 1.1 V. The SEU measurements for the part designed with lower operating voltage, 1.1 V is slightly larger than the one for the operating voltage of 1.3 V. This is similar to our new results for Motorola PowerPC 7448. Also, in figure 7 we compare the results of the SEU measurements of the D-Cache of the Motorola PowerPC 7455 with a core of 1.6 V with the results of the Motorola PowerPC 7455 with a core voltage of 1.3 V. Contrary to the results for Motorola PowerPC 7448 and results for PowerPC 7457, there is no change in the SEU cross section for D-Cache.

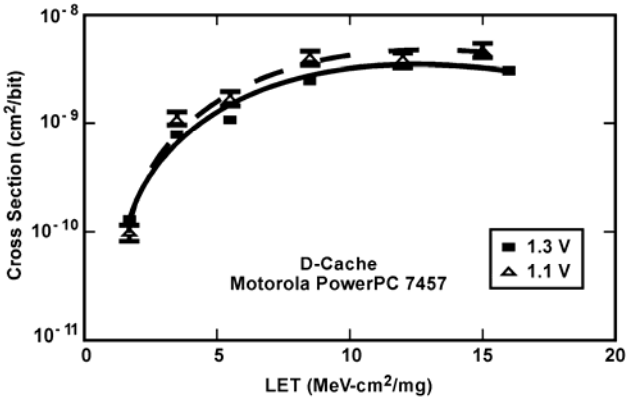

Fig. 6 Comparison of SEU cross sections for D-Cache for Motorola PowerPC 7457 with clock frequency of 400 MHz for internal core voltage of 1.3 and 1.1V. The dashed and solid curves are only guides for the eye.

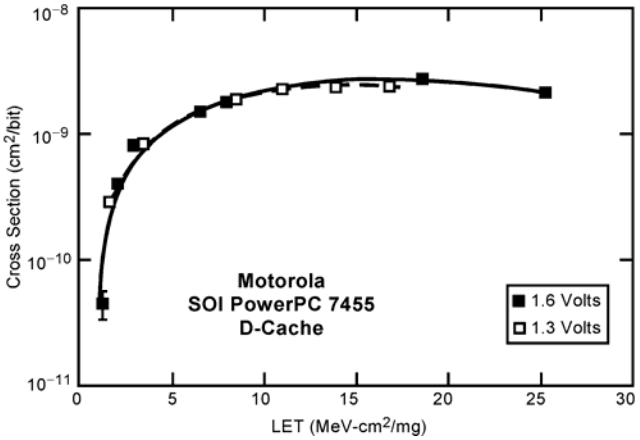

Fig. 7 Comparison of SEU cross sections for D-Cache for Motorola PowerPC 7455 with clock frequency of 800 MHz for internal core voltage of 1.6 and 1.3V. The dashed and solid curves are only guides for the eye.

These measurements for D-Cache suggest that the SEU sensitivity decreases with reduced core voltage up to a point where the trend reverses. For a particular feature size reduction of core voltage below 1.3 V increases the SEU sensitivity. The dependence of the SEU cross section with internal core voltage in SOI processors will be discussed further in Section IV.

B. Functional Errors ("Hangs")

Figure 8 compares estimated cross section for hangs for two internal core voltage specifications 1.3 and 1.0 V, during

heavy-ion SEU measurements of the Motorola PowerPC 7448 (90 nm feature size). It is interesting to note that the SEU hangs cross section for the parts designed with the lower operating voltage, 1.0 V, is larger than SEU hangs cross section for the part designed for operating voltage of 1.3 V by a about an order of magnitude.

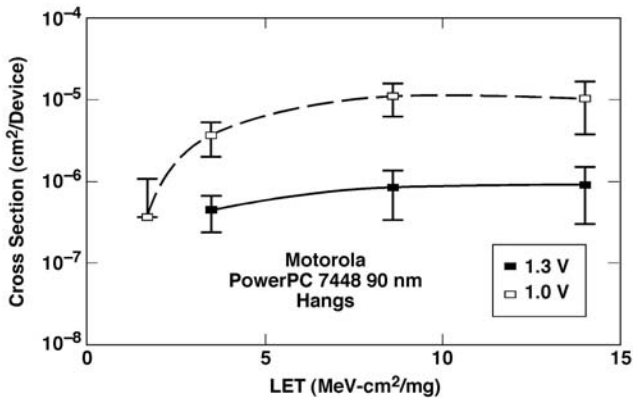

Fig. 8 Comparison of SEU cross sections for "hangs" for Motorola PowerPC 7448 for internal core voltage of 1.3 and 1.0V. The dashed and solid curves are only guides for the eye.

Figure 9 compares our previous results of the estimated cross section for hangs for the Motorola PowerPC 7455 with internal core voltage of 1.6 V to those for a special version of the Motorola PowerPC 7455 that operates with a low internal core voltage of 1.3 V. These data have been published previously [9]. Contrary to the new data for the Motorola PowerPC 7448, there is little difference between results of the two measurements.

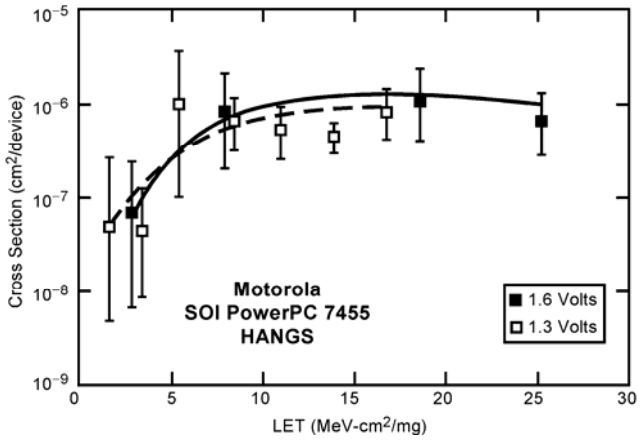

Fig. 9 Comparison of SEU cross sections for hangs for Motorola PowerPC 7455 with clock frequency of 800 MHz for internal core voltage of 1.6 and 1.3V. The dashed and solid curves are only guides for the eye.

IV. DISCUSSION

Feature sizes, silicon film thickness and internal core voltages are critical factors for single-event upset in SOI. Scaling for high-performance technologies depend heavily on reducing feature size, but also requires a reduction in internal core voltage [11]. The effect of scaling on partially depleted SOI structures is a far more difficult problem. The main advantage of SOI is a marked reduction in the thickness of the silicon region for charge collection. To first order, this should decrease the collected charge. However, charge amplification from the parasitic bipolar transistor that is inherent in partially depleted SOI increases the charge by a significant factor. Reduction in feature size and decreasing the silicon film thickness increases bipolar gain. Furthermore, considerable work has been done showing that the critical charge for SOI devices with low internal core voltages is expected to be lower for more highly scaled devices [12]. This might lead to the conclusion that SEU will be far more severe for highly scaled devices with lower internal core voltages. However, this has not been observed for high-performance devices such as microprocessors [13]. Other factors cause less charge to be collected as devices are scaled to smaller feature size. Charge collection may also be lower when feature sizes are reduced below about 250 nm because the lateral distribution of charge from the ion track will extend beyond the active area [14]. The decrease in critical charge is compensated for by a smaller area along with decreased charge collection efficiency.

Reduction in feature size and core voltage should reduce the SEU sensitivity. Decreasing the silicon film thickness increases bipolar gain, and reducing the internal core voltage limits the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors. Table III shows the feature sizes, film thickness, internal core voltages, and saturated cross section for the SOI and bulk generations of the PowerPC family.

Table III Comparison of the PowerPC Family of Advanced Processors.

Device	**Feature Size (nm)**	**Film Thickness (nm)**	**Core Voltage (V)**	**Cross Section (cm^2)**
Motorola 7455†	180	110	1.6	~$2.7x10^{-9}$
Motorola 7455†*	180	110	1.3	~$2.4x10^{-9}$
Motorola 7457†	130	55	1.3	~$2.4x10^{-9}$
Motorola 7457†*	130	55	1.1	~$4.6x10^{-9}$
IBM 750FX†	130	117	1.4	~$2.4x10^{-9}$
Motorola 7448†	90	40	1.3	~$9.2x10^{-10}$
Motorola 7448†*	90	40	1.0	~$1.1x10^{-9}$
Motorola 7400	200	Bulk	1.8	~$3.9x10^{-8}$
Motorola 750	290	Bulk	2.5	~$6.8x10^{-8}$

* Special low power version.

† SOI technology.

Silicon film thickness is a critical factor in SOI single-event upset. From the standpoint of electrical device design, there is a tradeoff between bipolar gain and the history effect (which causes switching waveforms to depend on previous switching waveforms). The history effect can be reduced by decreasing film thickness, but that increases bipolar gain. In Ref. 9, there is a comparison between SEU cross section for IBM 750FX and Motorola 7457. There is a very good agreement between the data. The similarity between D-cache results of the Motorola 7457 and IBM 750FX is somewhat surprising. The feature size and core voltage of two processors are the same. However, the film thickness of the Motorola 7457 is much smaller - 55 nm – compared to the 117 nm film thickness of the IBM 750FX. These results might suggest that scaling between 180 and 130- nm feature size has no change in bipolar gain sensitivity. This is in contradiction with the common belief that the bipolar amplification increases inversely with the film thickness. A similar conclusion is reported in [15]. Ref. 16 contributes reduction of supply voltage and reverse doping profile used for more advanced technologies to the degradation of the bipolar gain, in spite of decreasing film thickness.

The results for the Motorola PowerPC 7448 processor for 1.3 V internal core voltages, presented in this paper show lower D-Cache SEU cross section compared to the PowerPC 7455 and 7457. The cross section per bit is about 40% lower for the D-Cache in the Motorola PowerPC 7448 and a similar reduction in cross section was observed for the FPR at high LETs. These results suggest that scaling between 130 and 90 nm feature size has considerable effect on SEU sensitivity. However, this trend is not true for the hangs. There is good agreement between hangs data for the PowerPC 7455, 7457 and 7448 (Fig. 4) at internal core voltage setting of 1.3 V, despite the difference in feature size. These results might suggest that scaling between 180 and 90 nm feature size has little effect on hangs sensitivity as long as internal core voltage stays above 1.3V.

For the Motorola PowerPC 7455 with feature size of 180 nm, the data shows (Figs. 7 and 9) no significant difference in D-Cache and hangs occurring for internal core voltages of 1.3 and 1.6 V. However, for the Motorola PowerPCs 7457 and 7448 with feature size of 130 and 90 nm, respectively, the data shows (Figs. 5, 6 and 8) a significant difference in D-Cache and particularly in hangs for internal core voltages of 1.3, 1.1 and 1.0 V. The D-Cache SEU cross section for the Motorola PowerPC 7448 with an internal core voltage of 1.0 V is considerably larger that the one for 1.3 V. There is more drastic increase in hangs estimated cross section. The hangs for the Motorola PowerPC 7448 with internal core voltage setting of 1.0 V is about an order of magnitude larger that the one with internal core voltage setting of 1.3 V. This suggests that reduction of the internal core voltage beyond a limit causes the improvement in SEU for highly scaled SOI commercial PowerPC microprocessors to be reversed. Because of the trend in scaling, feature size and internal core voltage constantly decreasing, the concern about SEUs is becoming an important factor and it should be investigated in more detail.

Although it is useful and instructive to make comparisons of single-event upset results as microprocessors within a given family evolve, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that different processors in the series respond to radiation. There are also different requirements for various registers and functions within the device. For example, access time is a critical requirement for on-board cache, but cache single-event upset results may not be representative of other types of registers within the device.

V. Conclusion

This paper has evaluated SEU cross section for the Motorola PowerPC 7448 with feature size of 90 nm at internal core voltages as low as 1.0 V. At internal core voltage of 1.3 V the SEU cross section is lower by a factor of five compare to the results for PowerPCs with feature size of 130 and 180 nm. The threshold LET did not change compare to the results for PowerPCs with feature size of 130 and 180 nm. The SEU cross section increases at lower internal core voltage of 1.0 V compared to the results at internal core voltage of 1.3 V. More drastic results were obtained for estimated cross section for “hangs.” The estimated cross section is higher by more than an order of magnitude for the results at internal core voltage of 1.0 V.

The fact that SOI devices are dielectrically isolated, have reduced collection volume, and reduced p-n junction area as compared to bulk devices makes it possible to manufacture SOI devices with better SEU. The upset rates of the SOI PowerPCs are low enough to allow their use in space applications where occasional upsets can be tolerated. The upset rate in D-Cache is 20 per year from galactic cosmic rays in deep space. Although a small number of “hangs” were observed during radiation tests, the cross section for this type of functional error is low enough that “hangs are expected only occasionally, with an estimated rate of two in 25 years from galactic cosmic rays in deep space.

Further reduction in internal core voltage together with increases in clock frequency may become serious factors in the overall impact of SEU rates for future generations of commercial SOI microprocessors.

References

[1] G. M. Swift, F.F. Farmanesh, S.M. Guertin, F. Irom, and D. G. Millward, “Single-Event Upset in the Power PC750 Microprocessor,” IEEE Trans. Nucl. Sci., 48(6), pp. 1822-1827 (2001).

[2] R. Velazco, S. Karoui, T. Chapuis, D.Benezech, and L.H. Rosier, “Heavy Ion Test Results for the 68020 Microprocessor and the 68882 Coprocessor,” RADECS 91 Proceedings, pp. 445-449.

[3] F. Bezerra, et al., “Commercial Processor Single Event Tests,” 1997 RADECS Conference Data Workshop Record, pp. 41-46.

[4] D. M. Hiemstra and A. Baril, “Single-Event Upset Characterization of the Pentium MMX and Pentium II Microprocessors Using Proton Irradiation,” IEEE Trans. Nucl. Sci., 46(6), pp. 1453-1460 (1999).

[5] F. Estreme, et al., “SEU and Latchup Results for SPARC Processors,” 1993 IEEE Radiation Effects Data Workshop, pp. 13-19.

[6] A. Moran, et al., “Single Event testing of the INTEL 80386 and the 8046 Microprocessor,” RADECS95 Proceedings, pp. 263-269.

[7] J. P. Colinge, “Silicon-on-Insulator Technology: Overview and Device Physics,” 2001 IEEE Nuclear and Space Radiation Effects Conference Short Course, Vancouver, Canada.

[8] F. Irom, F. H. Farmanesh, A. H. Johnston, G. M. Swift, and D. G. Millward, “Single-Event Upset in Commercial Silicon-on-Insulator PowerPC Microprocessors,” IEEE Trans. Nucl. Sci. 49(6), pp. 3148-3155 (2002).

[9] F. Irom, F. H. Farmanesh, G. M. Swift, A. H. Johnston, and G. L. Yoder, “Single-Event Upset in Evolving Commercial Silicon-on-Insulator Microprocessor Technologies,” IEEE Trans. Nucl. Sci. 50(6), pp. 2107-2112 (2003).

[10] F. Irom, and F. H. Farmanesh, “Frequency Dependence of Single-Event Upset in Advanced Commercial PowerPC Microprocessors,” IEEE Trans. Nucl. Sci., 51(6), pp. 3505-3509 (2004).

[11] B. Davari, R.H. Dennard, G.G. Shahidi “CMOS scaling for high performance and low power-the next ten years,” Proceeding of the IEEE, 83(4), pp. 595-606 (1995).

[12] E. L. Peterson et al., “Calculations of Cosmic-Ray Induced Upset and Scaling in VLSI Devices,” IEEE Trans. Nucl. Sci., 49(6), pp. 2055 (1982).

[13] A.H. Johnston, “Radiation Effects on Advanced Microelectronics Technologies,” IEEE Trans. Nucl. Sci., 45(3), pp. 1339-1354 (1998).

[14] P. E. Dodd, “Device Simulation of Charge Collection and Single-event Upset,” IEEE Trans. Nucl. Sci. 43(3), pp. 561-575 (1996).

[15] V. Ferlet-Cavrois et al., “Characterization of Parasitic Bipolar Amplification in SOI Technologies Submitted to Transient Irradiation,” IEEE Trans. Nucl. Sci. 49(3), pp. 1456-1461 (2002).

[16] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, P.E. Dodd, “Radiation Effects in SOI Technologies,” IEEE Trans. Nucl. Sci., 50(3), pp. 522-538 (2003).